LEPECVD Provides High-Quality Virtual Substrates

for Ge-rich SiGe p-MOSFETs

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These days the vast majority of available SiGe products are based on the Hetero-Bipolar Transistor (HBT), with UHV-CVD as the established deposition technique for production. The HBT is produced either as a discrete device or combined with traditional Si CMOS technology in SiGe BiCMOS ICs. These integrated circuits, taking advantage of the superior electronic properties of SiGe and the low production costs of CMOS, are already rushing into the fast-growing wireless telecommunications market. Up to now, the primary role of the SiGe enhancement to Si CMOS ICs has been to add RF functionality that otherwise would have to be implemented with additional, expensive III-V-based devices.

SiGe CMOS

A technological route with even more significance than the BiCMOS communications segment is the introduction of the SiGe enhancement into the CMOS technology itself. The combination of thin, tensilely strained Si layers (for n-type MOSFETs) with thin, compressively strained Ge-rich layers (for p-type MOSFETs) leads to strongly enhanced electron and hole mobilities for the n- and the p-type devices respectively. This higher carrier mobility will ultimately enhance virtually all of the important electrical characteristics of the transistors. A successful implementation of a SiGe-based CMOS process could significantly boost the performance of this mainstream technology. If such an implementation adheres to some basic requirements for standard processes (lithography, wet and dry chemical processing, or even fundamental issues like mechanical substrate stability for easy wafer handling and – last, not least – availability of inexpensive substrates), it will give access to significantly higher performance levels at astonishingly low additional cost, as most of the processing steps will not change.

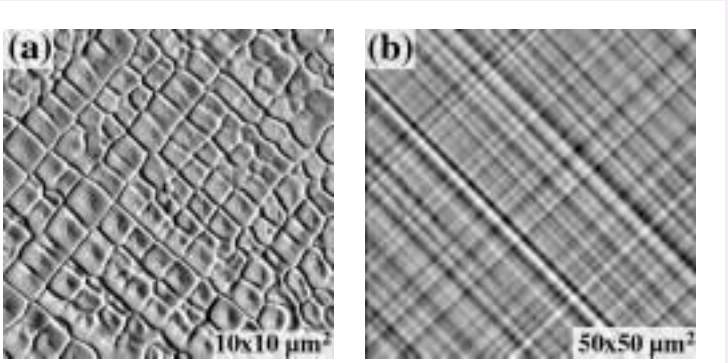

Figure 1: Pseudo-3D representations of AFM images obtained from virtual substrates with 70% Ge concentration before (a) and after (b) process sequence optimization. The troughs visible in (a) are as deep as 200 µm, while the maximum corrugation amplitude in (b) is less than 15 µm.

The main issue to be addressed for implementing SiGe CMOS, apart from the detailed design issues for the actual device heterostructures, is the production of substrates which can provide the strain needed for the active layers. Due to the relatively high mismatch between the lattice constants of Si and Ge of 4.2%, the strained, active layers have to be epitaxially deposited on some material with an intermediate lattice constant. One of the most promising approaches is to grow a thick, compositionally graded SiGe alloy buffer layer on a standard Si wafer, with the concentration increasing from pure Si to the Ge fraction needed for the desired mismatch. If the concentration gradient is shallow enough, the resulting virtual substrate will be fully relaxed and

sufficiently defect-free for the subsequent epitaxial deposition of the active transistor structures. The resulting requirements for very thick epitaxial layers and relatively low temperatures call for new approaches for the deposition processes. The development of LEPECVD at ETH Zurich in collaboration with NTB Buchs and Unaxis came just in time to address these issues.

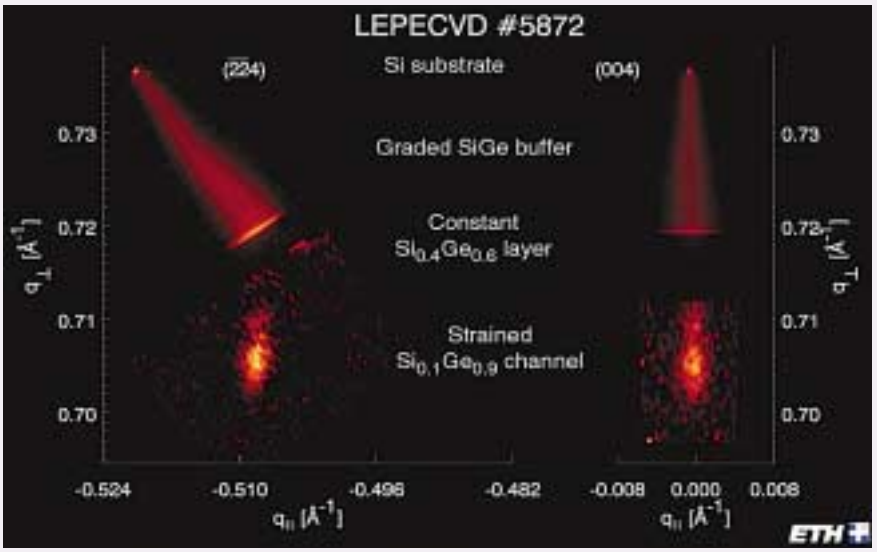

Figure 2: High-resolution X-ray diffraction reciprocal space map (HR-XRD RSM) around two Bragg peaks obtained from a complete p-MOSFET layer sequence fabricated with LEPECVD

Ge-rich virtual substrates and SiGe p-MOSFETs

Here we will present the latest advances achieved in the production of Ge-rich virtual substrates aimed at the implementation of SiGe p-MOSFETs. The first results obtained from a working high-performance SiGe p-MOSFET fabricated completely by LEPECVD and processed by DaimlerChrysler Research & Development in Ulm, Germany, showed a record hole mobility of more than 750 cm^2/Vs [1]. After these encouraging results, we used the 4" LEPECVD prototype and development system at ETH Zürich to further improve the structural quality of the virtual substrate with Ge concentrations starting from 50% and the Ge-rich active strained channel with concentrations up to pure Ge.

The issues to be dealt with at higher Ge concentrations for the virtual substrate are the reduction of surface roughness and the density of threading dislocations, while maintaining full relaxation of the film to the desired lattice constant. As for the strained channel, its interfaces have to be sharp, and it must be kept completely free of dislocations and strain-induced roughening. While for optimizing the performance the Ge concentration in the channel should be as high as possible, ideally pure Ge, it becomes increasingly difficult to keep this strained layer flat. The reason lies in the "softer" properties of Ge compared with Si. Its melting point (938°C) is considerably lower than that of Si (1410°C), which gives Ge a much stronger tendency to be elastically deformed upon application of strain at typical temperatures used for epitaxy.

The key both for optimizing the virtual substrate and the strained channels is a deposition process, which allows for a wide temperature range without degrading the film quality and with no significant reduction of the growth rate. Fortunately, this is exactly the strength of LEPECVD: as the energy needed for the growth reactions is almost completely supplied by a very intense plasma, LEPECVD is practically independent of temperature in a surprisingly large process window. This allows for the deposition of very thick (between 5 and 15 µm) virtual substrates at temperatures reaching down to 500°C at growth rates between 4 and 10 nm/s. By balancing the requirements for a low temperature to suppress surface roughening and the need for a sufficiently high temperature for asserting the full relaxation, we developed optimized process sequences suitable for virtual substrates of up to 100% Ge concentration. The effect of this optimization on the surface morphology is shown in *Figure 1*.

To verify the structural quality of the complete p-MOSFET structures, we made extensive use of high-resolution X-ray diffraction reciprocal space mapping. This method is ideally suited for examining the crystal quality, the composition, the strain state and the thickness of individual layers of complete device sequences. An example of such a measurement is shown in *Figure 2*, documenting the high structural quality of the (fully relaxed) virtual substrate and the (completely strained) active Ge-rich channel.

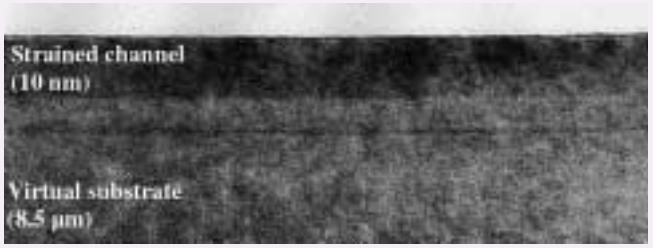

Figure 3: TEM image of the strained channel of a SiGe p-MOSFET structure. The channel contains 90% Ge and is grown on a 60% Ge virtual substrate.

In addition to the AFM and X-ray investigations, the shape and interface sharpness of the active, strained channel has been verified with transmission electron microscopy (TEM). As shown in *Figure 3*, we were able to obtain perfectly flat and abruptly defined Ge-rich channels by using appropriate process conditions.

The results of these optimizations are demonstrated again with the fabrication of transistor devices at DaimlerChrysler R&D. The obtained data are shown in *Figure 4*. The comparison concerns two important figures of merit, the saturation current and the maximum transconductance, of several transistors fabricated from three different structures. They have all been prepared by LEPECVD and consist of a strained Ge-rich channel of 80% or 90% Ge content on a virtual substrate with final Ge concentration of 50% and 60%, respectively. The data labeled "old" are from the devices of [1], where the other two SiGe devices have been obtained after the optimization of the deposition process sequence. As demonstrated, further research has paid off with a 30% – 40% enhancement for the 80% device, while the increase of the Ge concentration in the channel to 90% has boosted the performance by a factor of 2. In comparison to the Si reference device, it has to be stressed at this point that the only additional process step consisted of the LEPECVD epitaxy, which amounted to roughly 40 min!

Reference

[1] C. Rosenblad, Chip 4, 2001 (p. 24)

Dr. Matthias Kummer studied physics at the Swiss Federal Institute of Technology in Zuerich, Switzerland (ETHZ) from 1992 to1997 and received a diploma in Experimental Physics from ETHZ with an STM study of SiGe heteroepitaxial structures in 1998.
In 2001 Matthias Kummer received his PhD from the ETHZ with a thesis on the fabrication of device grade SiGe heterostructures grown with plasma-assisted techniques, in particular LEPECVD, in the group of PD Dr. Hans von Känel. While writing the PhD thesis he worked at the Interstate University for Applied Science of Technology in Buchs, Switzerland (NTB), in the Institute of Microsystem Technology with Prof. Alex Dommann, mainly on high-resolution X-ray diffraction analysis.

Figure 4: Comparison of the saturation current and the maximum transconductance for the transistors of [1] ("80% old"), a similar type obtained after optimization of the growth procedure ("80% new"), and a transistor with an active channel which contains 90% Ge ("90% new"). For comparison, a Si reference transistor is included in the plots.